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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,750	01/14/2004	Christopher A. Menkus	08211/0200349-US0/P05782	4265

38845 7590 06/21/2005

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,750	MENKUS, CHRISTOPHER A.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,15,18,20-23 and 25* is/are rejected.

7)☒ Claim(s) *4,6-14,16,17,19and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 5/18/05. Claim 4 has been amended. Claims 21 – 25 have been added. Claims 1 – 25 are pending on this application.

Response to Arguments

2. Applicant's arguments filed under remarks have been fully considered but they are not persuasive.

With respect to claim 1 and 20, under remarks, applicant argued that " no motivation to modify Myers as suggest by Wang from prior office action, because the circuit of Myers already resolves each measurement region into n different levels". Examiner respectful traverses from the following: Wang et al.; on Col 2 lines 13 – 15 clearly suggest that the fine channel that includes folding stages is to providing a finer measurement resolution, because each measurement region is resolve to n different levels. Even though, Myers already resolves each measurement into n different levels, however the suggestion of folding taught by Wang et al. will providing finer measurement resolution for each measurement region of Myers. Therefore, the motivation of "finer resolution measurement" for modifying of Myers by Wang et al. is proper.

With respect to claims 1 and 18, under remark applicant argued that "the combination of Myer and Nix et al. would change the principle of operation of Myer". Examiner respectful disagrees from the following:

The claimed invention drawing to a folding analog -to- converter comprising: a coarse channel calibration circuit, a coarse channel, and adjusting the parameter of the coarse channel from the calibration circuit. While Fig. 1 of Myer teaches an analog to digital converter having: coarse channel calibration circuit (11); a coarse channel (Q1); and adjusting the parameter (13) of the coarse channel (Q1) from the calibration circuit (11). Therefore the coarse channel (Q1) of Myers modify by the concept "folding coarse channel of Fig. 1 (120b)" taught by Nix to provide greater design flexibility with regard to resolution, power consumption, operation speed and cost. Accordingly, the modifying coarse channel of Myers et al. modify into folding coarse channel concept (120B taught by Nix has not thing to do of the principle operation circuit of Myers.

From above, the modifying of Myers teaches all limitation of the claimed invention. Therefore, the prior office action is applying to this office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 3, 5, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Myers U.S. Patent No. 5,184,127 in view of Wang et al. U.S. Patent No. 6,535,156.

Regarding claim 1, Fig. 1 of Myers discloses a circuit for analog-to-digital conversion (Col. 1 line 59), comprising: a fine channel circuit (Fine Quantizer Q2) that includes folding stages; a coarse channel circuit (Coarse Quantizer Q1); and a coarse channel calibration circuit (11) that is coupled to the coarse channel circuit (Coarse Quantizer Q1). However, Myers fails to disclose the fine channel circuit (Q2) includes folding stages.

Fig. 1 of Wang et al. discloses an analog-to-digital converter circuit (Col. 4 line 10) comprising: coarse channel (103); and fine channel (101) that includes folding stages (Col. 2 lines 8 – 13).

Myers and Wang et al. are common subject matter for Analog to Digital converter having coarse and fine channels. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the folding fine channel taught by Wang et al. into fine channel of Myers for the purpose to provide finer measurement resolution because each measurement regions is resolved to n different levels (Wang et al., Col. 2 lines13 – 15).

Regarding claim 2, Fig. 1 of Myers further comprising: a control circuit (Col. 4 lines 4 – 6 disclosing "External Circuitry" is controlling 11) that is configured to provide a select signal (Calibrate Enable); and a voltage reference circuit (13) that is configured to provide a voltage reference signal (output of 13) that corresponds to the select signal (Calibrate Enable), wherein the coarse channel circuit (Q1) is configured to receive the voltage reference signal (Col. 4 lines 19 – 25).

Regarding claim 3, Fig. 1 of Myers et al. further discloses wherein the coarse channel circuit (Q1) is configured to provide an output signal (Col. 4 lines 19 – 25) in response to a voltage reference signal (13), and wherein the coarse channel calibration circuit (11) is configured to: receive a feedback signal (Output of Q1 couple to 11) from the coarse channel circuit (Q1), and provide an adjustment signal (15) to the coarse channel circuit in response to the feedback signal (Col. 4 line 64 – Col. 5 line 9).

Regarding claim 5, Fig. 1 of Myers further disclose wherein the output signal includes the feedback signal (Fig. 1 disclosing the output signal of coarse channel Q1 is feedback to autocalibration microcomputer 11).

Regarding claim 20, the claim incorporated substantial the same subject matter as of claim 1, and rejected along the same rationale.

Regarding claim 22, wherein the coarse channel circuit (Q1) is arranged to perform a coarse analog –to-digital conversion, and wherein the coarse channel calibration circuit (11) is arranged to calibrate the coarse analog –to-digital conversion (Q1).

5. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Myers U.S. Patent No. 5,184,127 in view Nix et al. U.S. Patent No. 6,677,879.

Regarding claim 15, Fig. 1 of Myers discloses a circuit for calibration (11) in analog-to-digital conversion architecture (Col. 1 line 59) the circuit comprising: a coarse channel calibration circuit (11) that is configured to: receive an output signal from a coarse channel circuit (Output signal of Coarse Quantizer Q1) of analog- to-digital

converter circuit (Fig. 1) and adjust a parameter of the coarse channel circuit in response to the output signal (Col. 4 line 64 – Col. 5 line 6). However, Myers fails to disclose the analog-to-digital converter is a folding analog-to-digital converter.

Fig. 1 of Nix et al. discloses a folding analog-to-digital converter circuit (Col. 3 lines 62 - 63).

Myers and Nix et al. are common subject matter for Analog to Digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the folding analog-to-digital converter taught by Nix et al. into Myers's converter for the purpose of providing a repetitive output that varies over a particular input voltage range and provide greater design flexibility with regard to resolution, power consumption, operating speed and cost (Nix et al, Col. 1 line 61 – Col. 2 line 5).

6. Regarding claim 18, Fig. 1 of Myers disclose a method for coarse channel calibration (11) analog-to-digital conversion architecture (Col. 1 line 59); the method comprising: providing a reference voltage (13) to a coarse channel circuit (Coarse Quantizer Q1) of a analog-to-digital converter circuit (Fig. 1); and adjusting a parameter of the coarse channel circuit until an output of the coarse channel circuit is calibrated in relation to the reference voltage (See Fig. 2 from step 111- 125 for disclosing step 121 of adjustment for calibration process of Coarse Quantizer step 125 in relation to reference input at step 111). However, Myers fails to disclose the analog-to-digital converter is a folding analog-to-digital converter.

Fig. 1 of Nix et al. discloses a folding analog-to-digital converter circuit (Col. 3 lines 62 - 63).

Myers and Nix et al. are common subject matter for Analog to Digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the folding analog-to-digital converter taught by Nix et al. into Myers's converter for the purpose of providing a repetitive output that varies over a particular input voltage range and provide greater design flexibility with regard to resolution, power consumption, operating speed and cost (Nix et al, Col. 1 line 61 – Col. 2 line 5).

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Myers modify by Wang et al. as applied to claim 1 above, in further view of Tyrrel U.S. Patent No. 4,137,525.

Myers modify by Wang et al. as applied to claim 1 above, does not discloses wherein the coarse channel circuit includes an amplifier array.

Fig. 13 of Tyrrel et al. discloses an analog-to-digital converter having coarse channel circuit (468, 466) and fine channel circuit ((486, 488,494..); wherein the coarse channel circuit includes an amplifier array (468).

Myers modified by Wang as applied to claim 1, and Tyrrel are common subject matter for analog to digital converter having coarse and fine channels. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the amplifier array of coarse channel taught by Tyrrel into the

coarse channel of Myers for the purpose of providing an individual amplified signal from respective levels input signal (Col. 15 lines 31 – 33).

8. Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. U.S. Patent No. 6,535,156, in view of Myers U.S. Patent No. 5,184,127.

Fig. 2 of Wang et al. discloses a folding analog-to-digital conversion (Col. 1 lines 10), comprising: a coarse channel circuit (203, 204); a fine channel folding circuit (201, 202) that is arranged that is arranged to perform a fine analog to-digital conversion (201) of an input signal (input of 201) in parallel with the coarse analog-to-digital conversion of the input signal performed by the coarse channel circuit (input of 203). However, Wang et al. does not discloses a coarse channel calibration circuit that is configured to receive an output signal from the coarse channel and adjust a parameter of the coarse channel circuit in response to the output signal.

Fig. 1 of Myers disclose an analog to digital converter having a coarse channel calibration circuit (11) that is configured to receive an output signal from the coarse channel (Q1) and adjust a parameter (13, 15, 19) of the coarse channel circuit in response to the output signal.

Wang et al. and Myers are common subject matter for Analog to Digital converter having coarse and fine channels. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the calibration circuit (11) taught by Myers in to Wang et al. for the purpose of providing fast, accurate

conversion, low noise, and low distortion over the band width of interests (Col. 2 lines 11 – 17).

Allowable Subject Matter

9. Claims 4, 6 – 14, 16, 17, 19 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Respect to claim 4, prior arts fail to teach wherein the coarse channel circuit comprises an amplifier array and a comparator array, and wherein at least one of the amplifier array and the comparator array is configured to receive the adjustment signal.

Respect to claim 6, prior arts fail to teach wherein the coarse channel calibration circuit includes: a counter circuit that is coupled to the coarse channel circuit; and a parameter adjustment circuit that is coupled to the counter circuit and the coarse channel circuit.

Respect to claims 7 – 13, the claims either direct or indirect depending on object claim 6 above. Therefore the claims 7 – 13 are object for the same reason of claim 6.

Respect to claim 14, prior art fail to teach a control circuit that is configured to: provide a select signal and provide a timing signal at a pre-determined amount of time after providing the select signal, wherein the coarse channel circuit is configured to provide an output signal, and wherein the coarse channel calibration circuit is configured to latch the output signal in response to the timing signal.

Respect to claim 16, prior arts fail to teach a control circuit that is arranged to: provide a select signal for selecting a voltage reference; and assert a timing signal for latching the coarse channel calibration circuit at al pre-determined amount of time after a change of the select signal.

Respect to claim 17, prior arts fail to teach wherein the coarse channel calibration circuit includes: a counter circuit that is configured to provide a count signal in response to the timing signal and the output signal; and the parameter adjustment circuit that is configured to adjust the parameter in response to the count signal.

Respect to claim 19, prior arts fail to teach adjusting a count in response to the signal from coarse channel circuit; and wherein the parameter is adjusted according to the count.

Respect to claim 24, the claim direct depend upon an object claim 6 above. Therefore, the claim 24 is object for the same reason of claim 4.

Cited References

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are relating to coarse and fine analog-to-digital converter.

Conclusion

11. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

6/13/05

Linh Van Nguyen

Art Unit 2819

PEGUY JEANPIERRE
PRIMARY EXAMINER